Amendments to the Drawings

Amendments to FIGS. 1 and 3 on drawings sheets 1 and 3, respectively, are shown on the two annotated drawings sheets labeled "Annotated Sheet" appended hereto. Two corresponding replacement drawing sheets labeled "Replacement Sheet" are also appended hereto.

Remarks

Summary of Office Action

Claims 1-25 were pending in this application.

Claims 1-13* and 15-25 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 13 and 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Appleton et al., U.S. Patent No. 6,628,621 (hereinafter "Appleton").

FIG. 1 of the drawings is objected to pursuant to 37 C.F.R. § 1.84(o).

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* While the Examiner indicated that claim 1-12 and 15-25 are rejected under 35 U.S.C § 112, second paragraph on page 3 of the Office Action, a rejection of claim 13 under this section of the statute is included on page 4. Applicants therefore presume that the Examiner intended to indicate that claims 1-13 and 15-25 are rejected.

Summary of Applicants' Reply

Applicants have canceled claims 9-11, 23, and 24 without prejudice. Applicants reserve the right to pursue the subject matter of any of the canceled claims in one or more subsequent continuing applications.

Applicants have amended claims 1, 4, 13, 14, 21, and 22 to correct clerical and/or typographical errors and/or to more particularly define the invention. No new matter has been added and the amendments are fully supported and justified by the specification.

Applicants have added claims 26-33. No new matter has been added by the new claims and they are fully supported and justified by the specification.

Applicants have amended the specification to correct minor clerical and/or typographical errors. No new matter has been added.

Applicants have amended the drawings to clarify certain elements contained therein. No new matter has been added.

Applicants' reply to 35 U.S.C. § 112 rejections

With respect to claim 1, the Examiner contends that it is "unclear . . . how and interface would have a rate." Office Action, p. 3. Applicants have amended claim 1 to clarify the language in accordance with the Examiner's suggestion. The claim now recites "a bit error rate of a data transmission through an interface."

Also with respect to claim 1, the Examiner contends that the terms "comparison data" and "test data" are unclear. Contrary to the Examiner's contention, applicants respectfully submit that these terms are clearly defined in the specification. For example, at page 7, lines 21-25, the specification defines test data:

> When test data 130 is accessed and formatted (if necessary), test data stream 132 is transmitted by the above-described transmission circuitry to the interface on which bit error rate testing is being conducted.

The specification defines comparison data, at, for example, page 18, lines 18-27:

> Comparison data 134 corresponds to test data 130 and is used to determine if the data stream coming in from transceiver 102 contains any errors using the comparison circuitry. For example, comparison data 134 may be identical to test data 130. Otherwise, comparison data 134 corresponds to test data 130 in some suitable way such that it may be determined

> whether any errors occurred during the transmission process, and if so, how many.

The specification, therefore, makes is abundantly clear that comparison data is expected data and test data is the data used to test the data stream coming out of the interface. Because "[a]n applicant is entitled to be his or her own lexicographer . . . " (MPEP § 2111.01(III)), applicants respectfully submit that the terms "test data" and "comparison," as used in the claims, are not indefinite. Applicants therefore respectfully request that the rejection of claim 1 under 35 U.S.C. § 112, second paragraph, be withdrawn.

With respect to claim 3, the Examiner contends that "it is unclear . . . how a circuit would be implemented in a programmable logic device without using programmable logic circuitry." Office Action, p. 3. Contrary to the Examiner's contention, applicants respectfully submit that because programmable logic devices may include digital signal processing ("DSP") circuitry, various circuits may be implemented using DSP circuitry as opposed to programmable logic circuitry. As applicants' specification at, for example, page 14, lines 1-8 clearly states:

> Controller 112 may be implemented entirely in programmable logic. Alternatively, controller 112 may be at least partially implemented using

> hardwired digital signal processing ("DSP") logic (e.g., a microprocessor). Generally, any components of bit error rate tester 104 may be implemented entirely in programmable logic or at least partially implemented using hardware DSP.

Because it is clear how a circuit would be implemented in a programmable logic device without using programmable logic circuitry, applicants respectfully request that the rejection of claim 3 under 35 U.S.C. § 112, second paragraph, be withdrawn.

With respect to claims 9 and 10, because applicants have canceled these claims, their corresponding rejections are moot. However, claim 1 was amended to incorporate the feature of testing a data transmission through an interface that is internal to the programmable logic device. Therefore, applicant will address the Examiner's rejection under 35 U.S.C. § 112, second paragraph, of claim 9 with respect to amended claim 1.

The Examiner contends that "whether the interface is internal or external to the device[,] the functional equivalency would be unchanged." Office Action, p. 4. Applicants respectfully submit that, regardless of whether or not the "functional equivalency would be unchanged," this is

not a proper basis for rejection under 35 U.S.C. § 112, second paragraph.

With respect to claims 2-12 and 15-17, because the 35 U.S.C. § 112, second paragraph, rejection has been traversed with respect to claim 1, the inheritance of this rejection by the dependent claims has been traversed as well.

With respect to claim 13, the Examiner contends that the terms "comparison data" and "test data" are unclear. Applicants respectfully submit that this rejection should be withdrawn for at least those reasons discussed above with respect to claim 1.

With respect to claim 18, the Examiner contends that the phrases "synchronizing a comparison of incoming values with comparison values" and "comparing an incoming value to a comparison value" is unclear for the reasons stated with respect to claim 1. As discussed above with respect to claim 1, the specification defines what is meant by "comparison values" and "incoming values." Namely, data representing values coming into a comparator from an interface are compared to data representing values stored comparison data in order to determine whether there are any error in the incoming values.

Applicants therefore respectfully request that the rejection of claim 18 under 35 U.S.C. § 112, second paragraph, be withdrawn.

With respect to claim 21, the Examiner points out the repetition of step numbers relative to the base claim. Applicants have amended claim 21 to renumber the steps. Applicants therefore respectfully request that the rejection of claim 21 under 35 U.S.C. § 112, second paragraph, be withdrawn.

With respect to claims 19-21 because the 35 U.S.C. § 112, second paragraph, rejection has been traversed with respect to claim 18, the inheritance of this rejection by the dependent claims has been traversed as well.

With respect to claim 22, the Examiner contends that it is "unclear . . . how and interface would have a rate." Office Action, p. 5. Applicants have amended claim 22 to clarify the language in accordance with the Examiner's suggestion. The claim now recites "a bit error rate of a data transmission through an interface."

Also with respect to claim 22, the Examiner contends that the phrase "comparing the incoming data to the comparison data" is unclear. Applicants respectfully submit that the phrase has defined meaning for at least those reasons discussed with respect to claims 1, 13, and 18. Applicants therefore

respectfully request that the rejection of claim 22 under 35 U.S.C. § 112, second paragraph, be withdrawn.

With respect to claims 23 and 24, because applicants have canceled these claims, their corresponding rejections are moot. However, claim 18 was amended to incorporate the feature of testing a data transmission through an interface that is internal to the programmable logic device. Therefore, applicant will address the Examiner's rejection under 35 U.S.C. § 112, second paragraph, of claim 23 with respect to amended claim 18.

The Examiner contends that "whether the interface is internal or external to the device[,] the functional equivalency would be unchanged." Office Action, page 6. Applicants respectfully submit that, regardless of whether or not the "functional equivalency would be unchanged," this is not a proper basis for rejection under 35 U.S.C. § 112, second paragraph.

With respect to claim 25, the Examiner contends that the phrase "comparing the incoming data to the comparison data" is unclear. Applicants respectfully request that the rejection of claim 25 under 35 U.S.C. § 112, second paragraph, be

withdrawn for at least those reasons discussed above with respect to claims 1, 13, and 18.

Applicants' reply to 35 U.S.C. § 102(e) rejection

Claims 13 and 14 are rejected under 35 U.S.C. § 102(e) as being anticipated by Appleton. Applicant has amended claims 13 and 14.

Claims 13 and 14, as amended, are directed towards a method and a programmable logic device in which a bit error rate tester ("BERT") is implemented within the programmable logic device. The BERT tests the bit error rate of an interface that is internal to the programmable logic device. The use of a programmable logic device to test its own internal interfaces is beneficial in terms of, for example, cost savings. Applicants' invention attempts to overcome the need to use expensive dedicated equipment. Because many programmable logic devices have interfaces through which data flows on the order of gigabits per second, the dedicated equipment capable of handling such a throughput rate becomes increasingly expensive. Applicants' invention does away with the need for the expensive dedicated BERT by making use of the programmable logic device to test its own interfaces.

Appleton generally relates to a field programmable gate array that implements multiple BERTs in order test the bit error rate along multiple time division multiplexed communications channels on an external network communication frame.

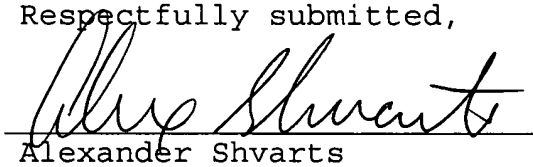
Applicants respectfully submit that nowhere in Appleton is there any mention or suggestion of using a programmable logic device to test the bit error rate of any data transmission through interfaces internal to the programmable logic device.

Therefore, applicants respectfully submit that claims 13 and 14 are allowable over Appleton. Claims 1-8, 12-17, 22, and 25-33 are allowable over Appleton for at least those reasons claims 13 and 14 are allowable over Appleton.

Conclusion

In view of the foregoing, applicants respectfully submit that this application is in condition for allowance. Accordingly, prompt reconsideration and allowance are respectfully requested.

Respectfully submitted,



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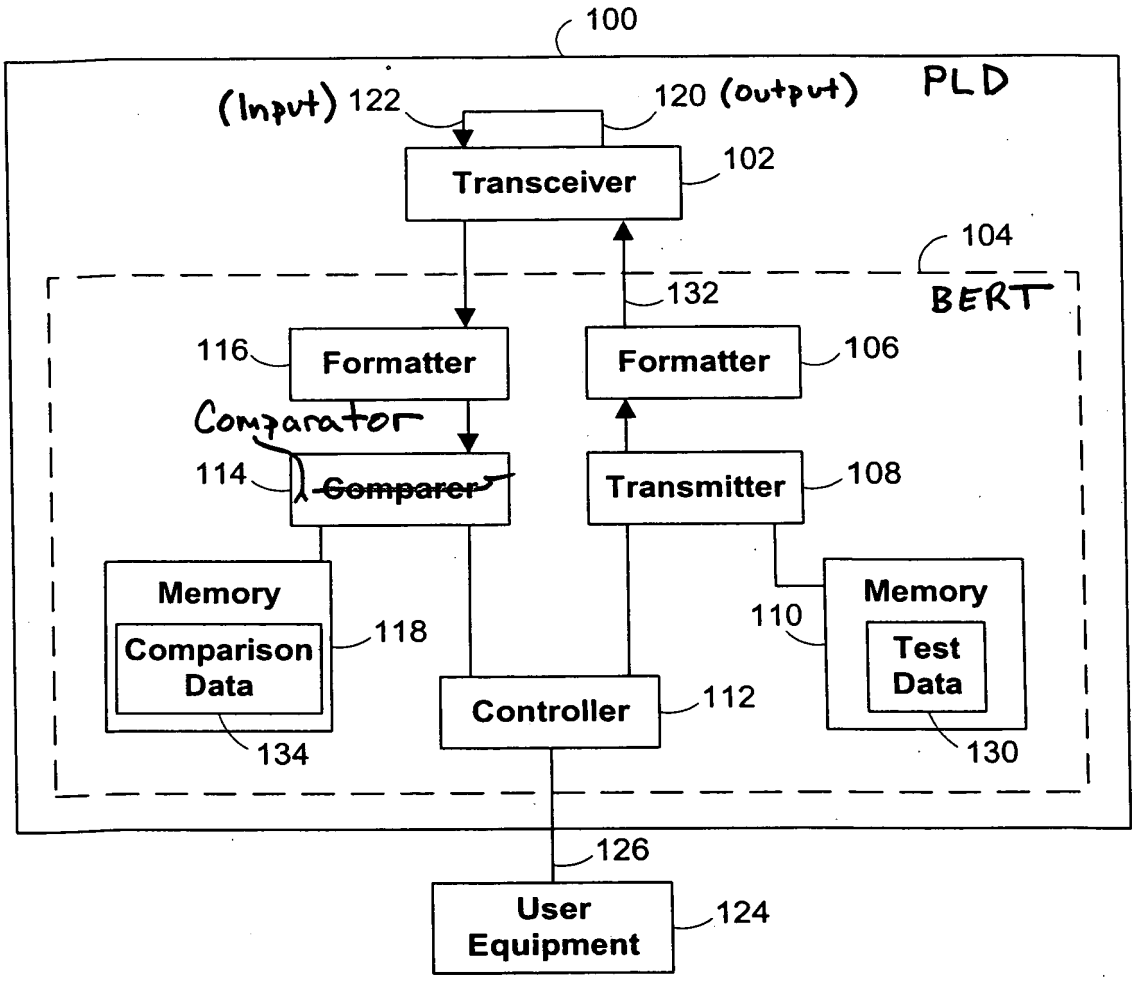

FIG. 1

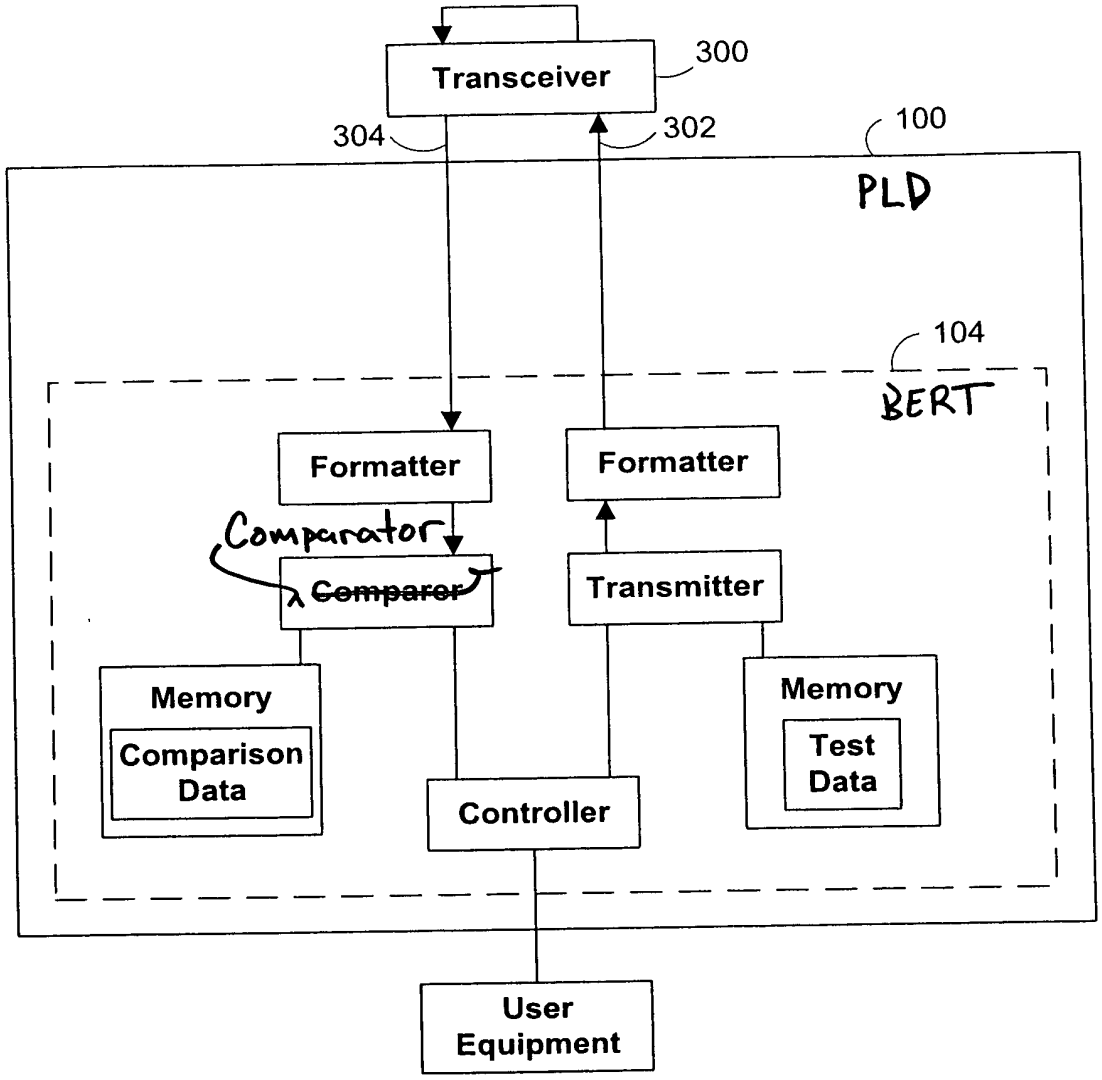
Transceiver
300
304
302
100
PLD
104
BERT
Formatter
Formatter
Comparator
Comparer
Transmitter
Memory
Comparison Data
Memory
Test Data
Controller
User Equipment

FIG. 3